Application No.: 10/593,280

REMARKS

In view of the following remarks, Applicants respectfully submit that all claims of the instant application are in condition for allowance, an indication of which is respectfully requested.

Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 2-14 would be allowable if rewritten in independent form. Applicants respectfully submit that claim 1 is also allowable over the cited prior art.

Specification

The abstract of the instant application was objected to for purported informalities. The abstract of the instant application has been amended. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication Number 2001/0049809 ("Miyauchi"). Applicants traverse this rejection for at least the following reasons.

Claim 1 recites a path memory circuit for use in a Viterbi decoding process performed based on state transitions through a number n (n is a positive integer) of states. The path memory circuit includes M (M is a positive integer) stages of storage circuits. Each storage circuit includes n rows of selective storage circuits. Each selective storage circuit includes a

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selection circuit for selectively outputting an input according to a result of the Viterbi decoding and a storage element circuit for storing a result selectively outputted from the selection circuit.

The path memory circuit includes a memory area A formed by the storage circuits of the first to i^{th} (i is an integer from 0 to M) stages; a memory area B formed by the selective storage circuits that select and hold a decoding result for any state k (k is an integer from 1 to n) of the storage circuits from the $i+1^{th}$ stage to the M^{th} stage; and a memory area C formed by the selective storage circuits other than the memory area A and the memory area B. According to a memory length control signal, the storage circuits of the j (j is an integer from i+1 to M)th and subsequent stages in the memory area C are stopped, and the selection circuits of the j^{th} and subsequent stages in the memory area B select an output of the selective storage circuits of a preceding storage circuit belonging to the memory area B.

To illustrate one non-limiting example, FIG. 4 of the instant application shows a path memory circuit that includes a memory area A (1), a memory area B (2), and a memory area C (3). *See*, Published Application at paragraph [0059]. The path memory circuit also includes a selective storage circuit 12. *Id.* The selective storage circuit 12 includes the selection circuit 10 and the storage element circuit 11. *Id.* The memory area A is an area including the selective storage circuits 12 for all the states up to the i^{th} stage, which are needed when the Viterbi decoding results converge at the earliest point in time. *See*, Published Application at paragraph [0061]. The memory area B is an area including selective storage circuits 12 from the $i+1^{th}$ stage to the M^{th} stage (e.g., for stage 0). *Id.* The memory area C is an area including all the other selective storage circuits 12. *Id.*

Applicants respectfully submit that Miyauchi fails to describe or suggest a path memory circuit that includes a memory area A formed by the storage circuits of the first to i^{th} (i is an

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integer from 0 to M) stages; a memory area B formed by the selective storage circuits that select and hold a decoding result for any state k (k is an integer from 1 to n) of the storage circuits from the $i+1^{th}$ stage to the M^{th} stage; and a memory area C formed by the selective storage circuits other than the memory area A and the memory area B, wherein according to a memory length control signal, the storage circuits of the j (j is an integer from i+1 to M)th and subsequent stages in the memory area C are stopped, and the selection circuits of the j^{th} and subsequent stages in the memory area B select an output of the selective storage circuits of a preceding storage circuit belonging to the memory area B, as recited in claim 1 (emphasis added).

The Office Action points to FIG. 2 of Miyauchi as allegedly showing this feature. *See*, Office Action at page 3. Miyauchi, in FIG. 2, shows arrangement of the memory cells in the path memory in the register transition method. However, the alleged arrangement does not show a memory area B and a memory area C, in a manner recited in claim 1. For example, the alleged arrangement does not show a memory area B including selective storage circuits from the $i+1^{th}$ stage to the M^{th} stage. *Id.* Similarly, the alleged arrangement does not show a memory area C formed by the selective storage circuits other than the memory area A and the memory area B.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1.

Conclusion

Accordingly, it is believed that the application is now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or

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an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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